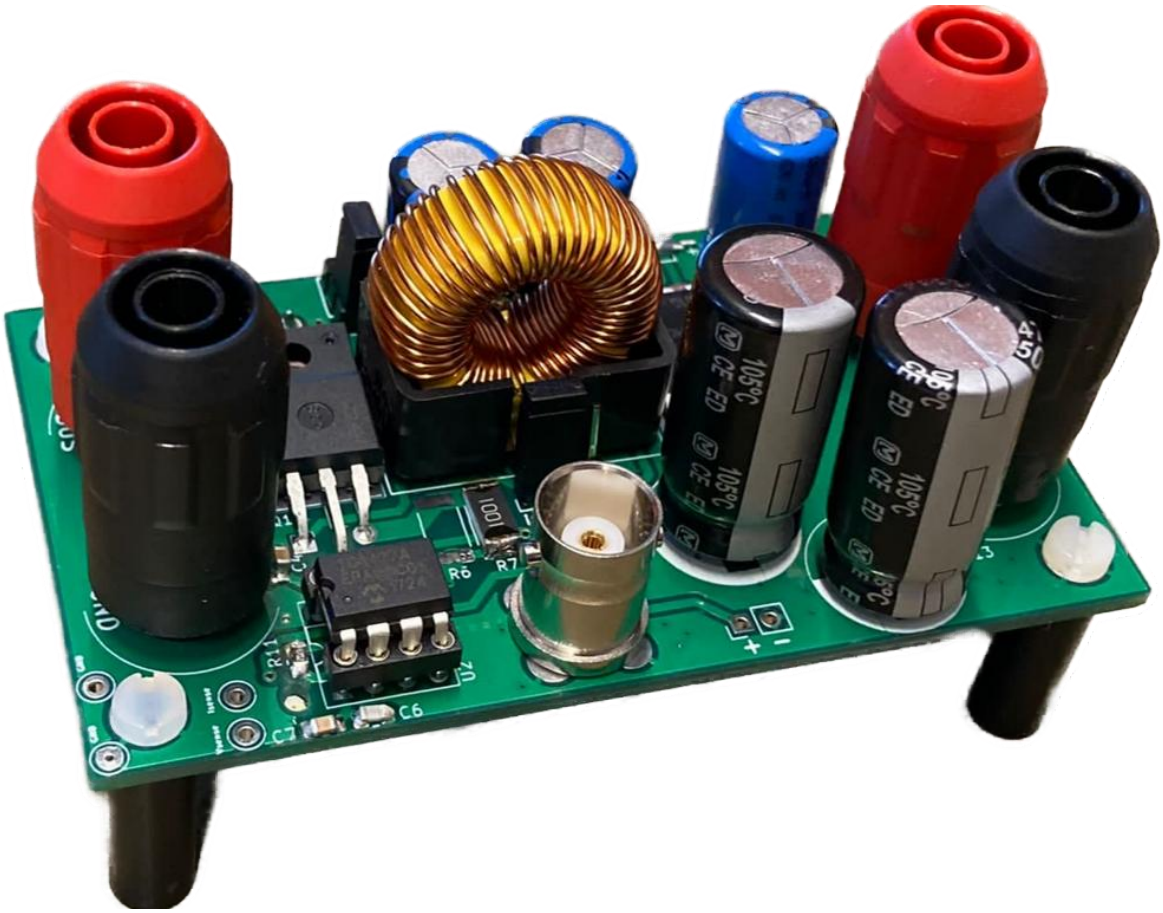
POWER ELECTRONICS



Elektrische **Om**zettingen en **Vo**edingen
ELOMVO 2026-2027

Final V1.4

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DC POWER LABORATORY

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Course Information – ELOMVO

- **Collaboration:** Students may work and discuss in pairs. Groups of more than two students are not permitted.

- **Laboratory structure**: The laboratory course consists of seven sessions over seven weeks. Each session corresponds to a chapter number, allowing you to monitor whether you are on schedule.

- **Reporting:**
    - Each student must prepare and submit an individual report.
    - The cover page must include your name, student number, collaboration partner and submission date, and all must be professionally formatted.
    - You may choose your own layout, but the final report must be clear and professional. Apply the reporting techniques taught in the program, page numbers, picture descriptions, etc.
- **Report content:**
    - Complete all tables digitally.
    - Insert screenshots and photographs correctly and ensure that all details are clearly legible.
    - For every simulation, include a screenshot followed by your explanation and findings.
    - Save oscilloscope screenshots directly to a USB drive using Save Image. Handwritten readings and unclear photographs of the oscilloscope display will not be assessed.
- **Software: Use CASPOC for simulations.**
    - Download it from: https://dc-pe.org/hhs/ve/Caspoc2015Praktikum.zip
- **Submission:**
    - Submit the complete report through Brightspace during the final week of the laboratory course, no later than Sunday at 23:59.
    - The submission folder will be made available in advance.
- **Checks and attendance:**
    - The lecturer will perform interim checks during the classes. Always keep your complete report and measurement evidence available during classes.
    - Attendance is compulsory.
- **Finally:** Power electronics offers much more to explore than can be covered in this introductory laboratory course. If you are interested in a topic beyond the assignments, ask during the lesson; we are happy to discuss it.

Table of Contents

1 CASPOC Power Converter Simulations (WEEK 1)

1.1 Introduction to CASPOC Desktop

CASPOC is a specialized simulation environment for power electronics and allows you:

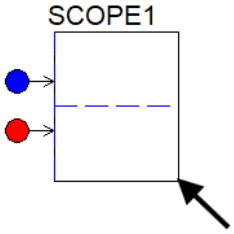
- Model circuits containing MOSFETs, diodes, inductors and capacitors.
- View current and voltage waveforms in real time.
- Simulate both open-loop and closed-loop control systems.
- Obtain results quickly without the convergence problems commonly associated with SPICE-based tools.
- Combine complex systems, such as converters with motor loads, in a single model.

In this laboratory course, CASPOC is used to investigate the operation of a boost converter. Download the latest course version from: https://dc-pe.org/hhs/ve/Caspoc2015Praktikum.zip
Extract the files to a folder on your drive and run Caspoc2017.exe

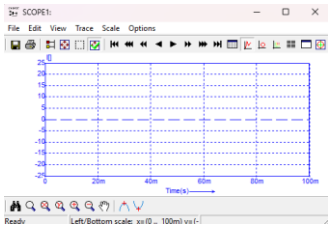
Taking measurements in CASPOC

Always measure currents using a scope. Moving the pointer over an inductor shows only the instantaneous current. The scope displays numerical values, maxima, minima, RMS values and average values at the bottom of the window.
Right-click the scope and use the arrow keys to inspect individual values.

Adding a scope



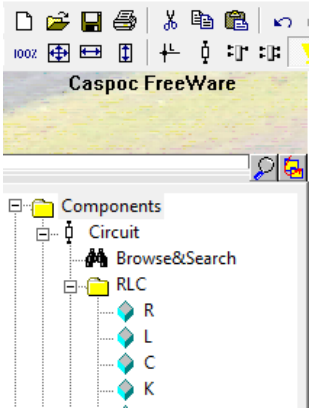
Right-click



A blue circular connection point indicates a current measurement. Drag it onto a component. To measure a voltage, draw a line from a circuit node to the connection point; it then changes into a square. Drag the bottom-right corner of the scope to enlarge it and reveal additional measurement inputs.

Adding components in CASPOC

Add components through the component library. If a component is difficult to find, enter its name in the search field above Components and select the magnifying-glass icon.



Additional controls

Use the Run button to start the simulation.

Use Simulation Time to change the simulated duration.

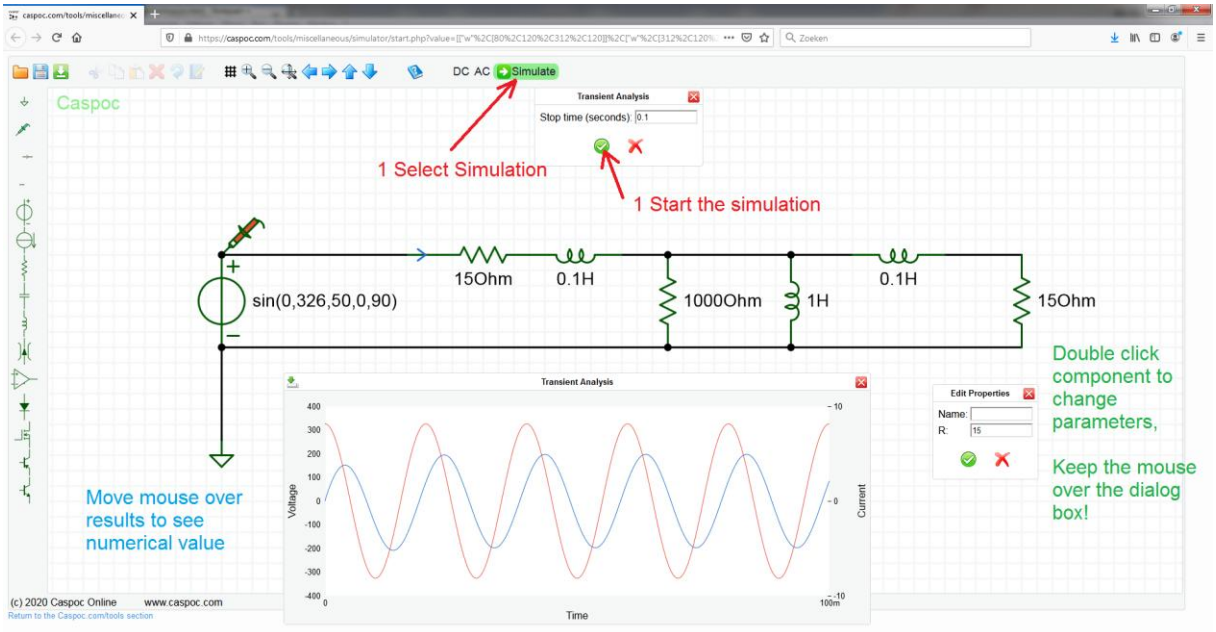
Use Animation to animated currents and operating states.

Use View to return the circuit to the center of the workspace.

1.2 Introduction to Caspoc Online

This is an introduction of the simplified CASPOC online environment, which requires little processing power and runs on a laptop, tablet or phone. The complete circuit is encoded in the URL, making a simulation easy to share.

Open the online tool at: https://dc-pe.org/hhs/onlinesim/#smps



If any difficulties occur with installing Caspoc Desktop the Caspoc Online tool can be used for the assignments. But you need to make the circuits yourself based figures of the models in this course document.

1.3 Introduction to the Boost Converter

What is a boost converter?
A boost converter (step-up converter) is a widely used DC-DC converter that produces an output voltage higher than its input voltage. For example, it can raise the 3.7 V supplied by a battery to 12 V or 24 V.
Its fundamental operating principle is based on temporarily storing energy in an inductor and subsequently transferring that energy to the output through a diode. Switching the MOSFET controls the storage and release of energy.

Typical applications:
- Power supplies for portable equipment.
- Solar converters and maximum power point tracking (MPPT).
- Automotive electronics, including 12 V to 24 V systems.
- LED drivers and battery chargers.

Basic circuit and operation
The principal components are:
- **Inductor (L): temporarily stores energy in a magnetic field.**
- **MOSFET (Q): acts as a switch that periodically connects the inductor to ground.**
- **Diode (D): conducts the stored energy to the output when the MOSFET is off.**
- **Capacitor (C): stabilises the output voltage and reduces voltage ripple.**

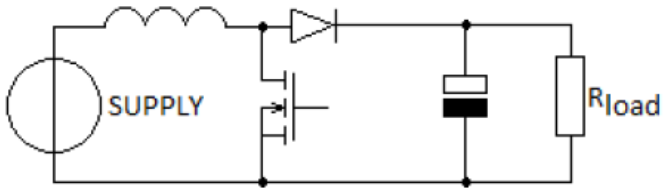


Figure 1.3.a – Schematic representation of a boost converter

Operation in two switching states:
1. **MOSFET on:** The inductor stores energy and its current increases. The diode is reverse-biased, while the output capacitor supplies the load.

2. **MOSFET off:** The inductor transfers energy through the diode to the output. The inductor voltage is added to the input voltage and supplies the load.

The inductor, diode and MOSFET form the power stage of the boost converter, as shown in Figure 1.3.a. A practical switched-mode power supply also requires a circuit that generates the MOSFET gate pulses. Changing the duty cycle of this pulse signal changes the output voltage. The gate signal may be generated by a function generator, an analogue controller or a microcontroller.

Open-Loop Boost Converter

In an open-loop system (Figure 1.3.b), the MOSFET is driven with a fixed duty cycle. The output voltage and current are not fed back to the controller.

- Advantage: simple and well suited to learning the basic operating principle.
- Disadvantage: the output voltage is not regulated and changes with the load or input voltage.

Practical example: a function generator driving the MOSFET at a fixed 50% duty cycle.

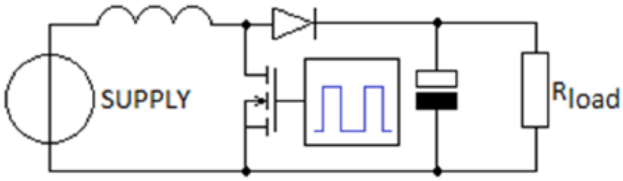


Figure 1.3.b – Open-loop control using a function generator

Boost Converter Conduction Modes

Depending on the selected components and operating conditions, the converter may operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). In CCM, the ideal average output voltage is calculated using:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D}$$

where:

- Vout = output voltage
- Vin = input voltage
- D = duty cycle (0 < D < 1)

A higher duty cycle produces a higher ideal output voltage.
In DCM, the relationship is more complex and depends on the inductance, load and switching frequency. At this stage, you only need to recognise that the inductor current may fall to zero at light load or with a small inductance, changing the converter behaviour.

1.4 Boost Converter Simulation

In this assignment, you will simulate a boost converter using CASPOC.

Step 1 - Open the model

Open the CASPOC model shown in Figure 1.4 (lesson1\boost.csi). - The input source V1 is set to 20 V DC.

- The function generator connected to the MOSFET gate is set to 50 kHz.
- The MOSFET is controlled by a pulse generator with a variable duty cycle.

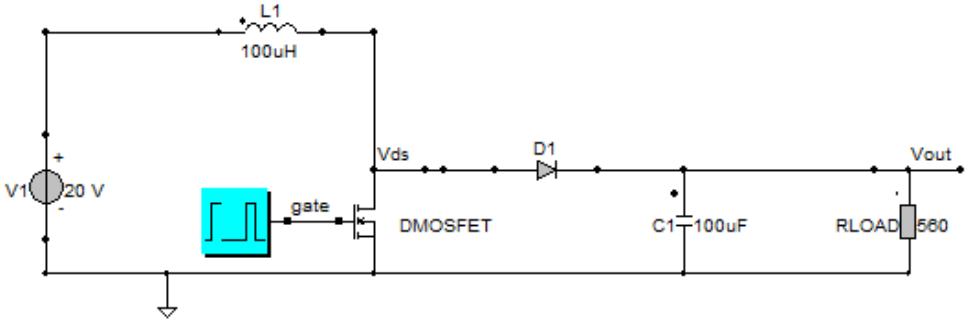


Figure 1.4 – Boost converter simulation model (boost.csi).

Step 2 - Vary the duty cycle
Set the duty cycle to 10%, 20%, 40%, 50% and 75%. For every duty cycle, measure the steady-state output voltage Vout for each of the three loads.

Duty cycle (%)	Vout (V)		
	No load RLOAD = 1 Mohm	Medium load RLOAD = 560 ohm	Heavy load RLOAD = 56 ohm
10			
20			
40			
50			
75			

Enter the steady-state output voltages in the table.

Step 3 - Analyse the waveforms
Create a scope plot and analyse: - Voltages: Vin, VDS and Vout. - Currents: inductor, MOSFET and diode currents. Demonstrate Kirchhoff's current law at the switching node and verify the inductor relationship uL = L di/dt using values from your own waveforms.

Step 4 - Capture evidence
- Include at least one screenshot for each load. - Set the displayed time interval to 1 ms. - Ensure that at least one complete switching period is clearly visible. - Place each screenshot directly beside the corresponding explanation. - The image must show the relevant scales and signal names.

Step 5 - Write a conclusion
Conclude the assignment in your own words. Explain how duty cycle and load affect the output voltage, identify Kirchhoff's current law and uL = L di/dt in your measured waveforms, and state whether the results agree with theory. Support every claim with a value or feature from your own simulation.

1.5 Buck Converter Simulation
In this assignment, you will investigate a buck converter using CASPOC.

Simulation at different duty cycles
Open lesson1/buck.csi and save a working copy so that the original model remains unchanged.

- Set the duty cycle to 10%, 25%, 50%, 75% and 90%.
- Run the simulation and record the measured results.
- Compare the measured output voltages with the theoretical values of Vout.

Parameters to determine:

- $V_{out,th}$: theoretische uitgangsspanning
- V_{peak}: hoogste spanning (piekniveau)
- t_{Vpeak}: tijdstip waarop de piek optreedt
- $V_{stationair}$: stationaire waarde van de spanning
- I_{peak}: hoogste stroomwaarde
- t_{Ipeak}: tijdstip van de stroompiek
- $I_{stationair}$: stationaire stroomwaarde
- $t_{settling,5\%}$: tijd die nodig is om binnen 5% van de stationaire waarde te komen

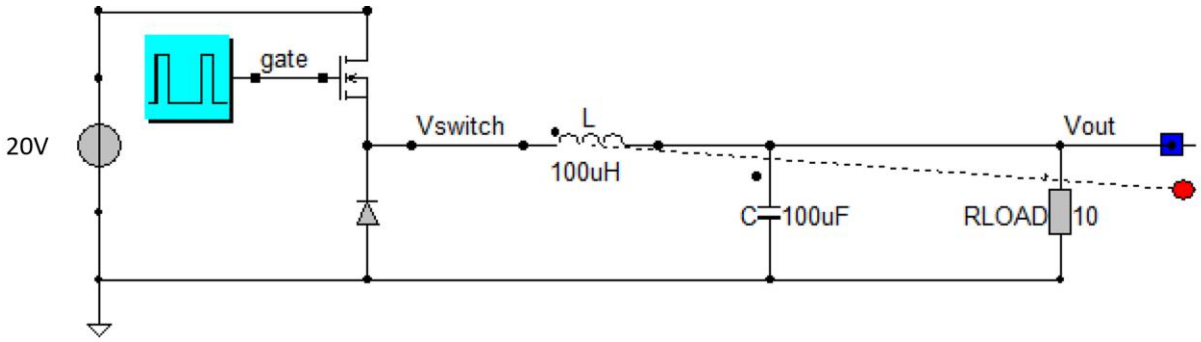


Figure 1.5 – Buck converter simulation model (buck.csi)

D	$Vout_{th}$ [1]	V_{peak}	t_{Vpeak}	Vsteady state	I_{peak}	t_{Ipeak}	Isteady state	$t_{settling\ 5\%}$
10%								
25%								
50%								
75%								
90%								

Complete the table by calculating the theoretical value of Vout and reading the other quantities from the graphs. For a signal with a final value of 100, the 5% settling time is the time required to enter the range from 95 to 105 and remain within that range. **Fout! Verwijzingsbron niet gevonden.**

Use the scope and arrow keys to inspect the results. Right-click a waveform to read a value directly. Press ENTER to continue the simulation from the point at which it stopped when a longer time interval is required.

1.6 Continuous Conduction and Duty Cycle

Use the circuit in Figure 1.5 (buck.csi) and determine the range of RLOAD for which the converter operates in continuous conduction mode at each duty cycle. Record your findings in the table.

D	R_{LOAD}
10%	< R_{LOAD} <
25%	< R_{LOAD} <
50%	< R_{LOAD} <
75%	< R_{LOAD} <
90%	< R_{LOAD} <

1.7 Inductive Load

Use the circuit in Figure 1.5 (buck.csi) and set the duty cycle to 10%. In steady state, the converter operates in DCM. Determine the inductance at the CCM/DCM boundary.

Compare the parameters in the table for Figure 1.3.4 with the new values. Explain why changing L changes the conduction mode and waveform.

1.8 Power

Use the circuit in Figure 1.5 (buck.csi) and set the duty cycle to 50%.
Measure the average input current.
Measure the average output current.
Calculate input and output power. Explain any difference between them.

1.9 Kirchhoff's Current Law

Use the circuit in Figure 1.5 (buck.csi) and set the duty cycle to 50%.
Measure the average inductor current.
Measure the average MOSFET current.
Measure the average diode current.
Show whether these values can also be derived from the measured input and output currents.

1.10 Transient Response

Continue the buck converter simulation by pressing ENTER until the inductor current is periodic and its maximum and minimum no longer change.
Measure the maximum and minimum inductor current.
Measure the time required for the inductor current to rise from its minimum to its maximum.
Calculate di/dt from these three measured quantities.
Use the measured di/dt and the converter voltages to calculate the inductance. Compare the result with 100 uH and explain the difference.

1.11 Conclusion

Summarise your main findings from Chapter 1 in your own words. Refer to your own calculated and simulated values. During the lesson, you may be asked to explain one of these findings orally.

2 CASPOC Closed Loop Converter (WEEK 2)

In a closed-loop converter, the output voltage or output current is continuously measured and compared with a reference value. A controller automatically adjusts the duty cycle to keep the controlled quantity close to its required setpoint. The general structure of a closed-loop converter is shown in Figure 2.

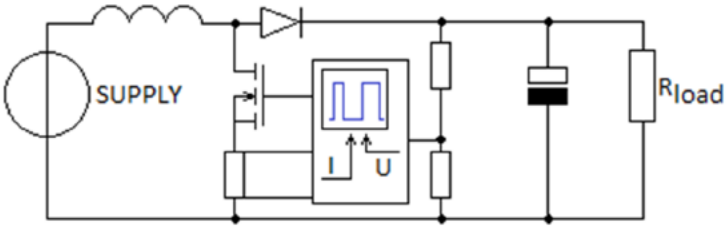


Figure 2 – General structure of a closed-loop converter

Advantages:

- stable and reliable output voltage or current;
- automatic compensation for changes in input voltage and load;
- improved regulation compared with open-loop operation.

Applications:

- laptop adapters and USB chargers;
- LED drivers;
- laboratory power supplies;
- industrial DC power supplies;
- battery chargers and renewable-energy converters.

Disadvantages:

- increased circuit complexity;
- a feedback network is required;
- the controller and feedback loop must be designed and compensated correctly;
- an incorrectly designed control loop can become unstable.

A practical example is a laptop adapter that maintains an output voltage of approximately 19V despite changes in mains voltage or load current.

2.1 Closed Loop Current Mode Controller Simulation

The file **Opbouw-Tut2-varfreq.csi** contains the components required to build the examples in this chapter, except for the required resistors and capacitors.

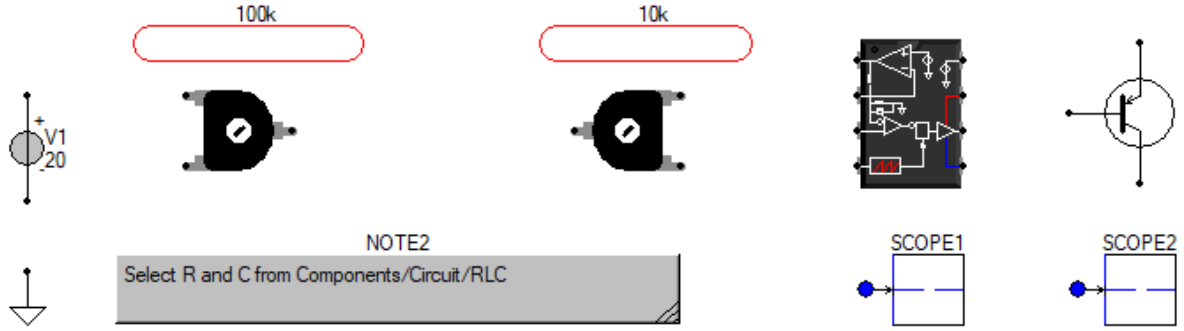


Figure 2.1.a – Example of the file opbouw-Tut2-varfreq.csi

Use the following filename format to save you own simulation model, ClosedLoop_personal-unique-code: **ClosedLoop_12345678.csi**

The resistor and capacitor components must be selected from:
Components → Circuit → RLC

The completed variable-frequency and variable-duty-cycle oscillator is shown below as a reference. Use the circuit topology as a guide, but construct and connect the simulation yourself.

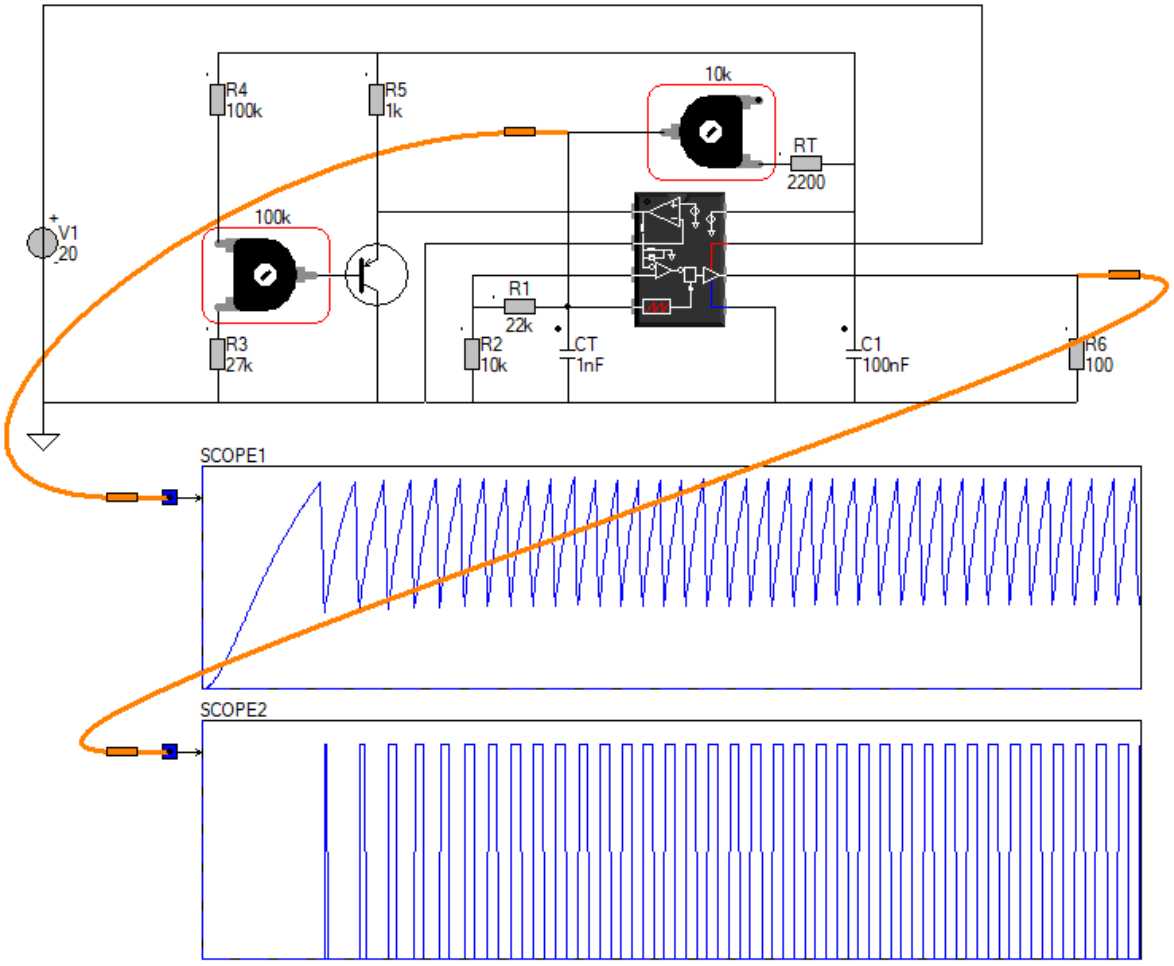


Figure 2.1.b – Variable-frequency and variable-duty-cycle oscillator in CASPOC

Construct the complete variable-frequency and variable-duty-cycle oscillator in CASPOC using the components supplied in **Opbouw-Tut2-varfreq.csi**. Add the missing resistors and capacitors and enter the required component values. Carefully check every connection before starting the simulation.

The lecturer will provide a unique code during the lesson. Enter this code in the **NOTE2** component and position the note in the top-left corner of the CASPOC schematic. The unique code must be entered in CASPOC before taking the screenshot. It may not be added or changed afterwards.

2.2 Closed Loop Simulation Schematic Evidence

Take a full-screen screenshot of the completed CASPOC schematic.
The screenshot must clearly show:

- the complete oscillator circuit;
- all connections;
- all component reference designators;
- all resistor and capacitor values;
- the CASPOC filename;
- the unique code in the NOTE2 component;
- the NOTE2 component positioned in the top-left corner.

Add the screenshot to your report as: **Figure 2.2 –** Completed schematic evidence.

Submit the corresponding original .csi simulation file together with your report. A screenshot without the corresponding simulation file is insufficient.

2.3 Closed Loop Simulation Waveforms Evidence

Run the completed CASPOC simulation (just like Figure 2.1.b) and display the following signals simultaneously:

- the oscillator sawtooth waveform in **SCOPE1**;
- the PWM pulse output in **SCOPE2**.

Adjust the scope settings so that at least five complete switching periods are clearly visible. The horizontal time scale of both scope windows must be identical so that the relationship between the sawtooth waveform and PWM pulse can be evaluated.
The lecturer's unique session code must remain visible in the top-left corner of the CASPOC schematic. Take a full-screen screenshot showing:

- the complete relevant schematic;
- the unique code;
- the sawtooth waveform in SCOPE1;
- the PWM pulse output in SCOPE2;
- clearly readable time and amplitude scales;
- at least five complete switching periods.

Add the screenshot to your report as: **Figure 2.3 –** Complete Waveforms Evidence.

3 The UC384x Current-Mode IC on a Breadboard (WEEK 3)

In this chapter, you will investigate the functions of the UC384x current-mode controller. The 'x' tells what behavior this version of the IC has. You will build and test the circuits shown using a breadboard.

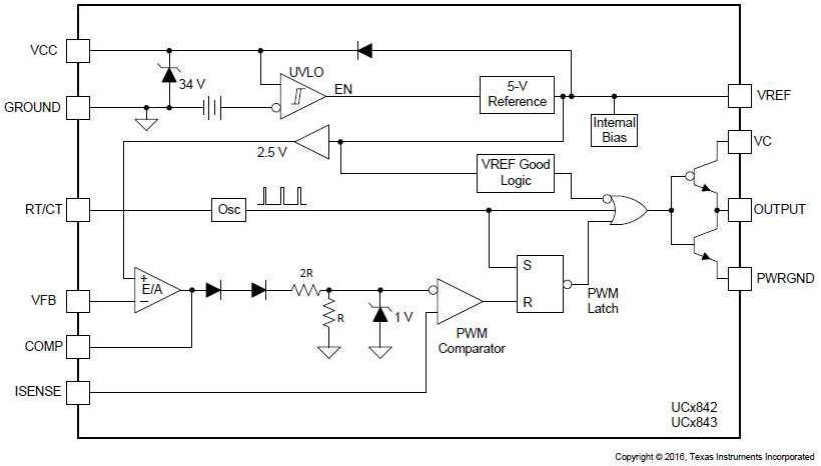


Figure 3.a – Functional block diagram of the UC3842

The pin layout of the IC is shown in **Figure 3.b**. The pin layout is the same for both the PDIP and SOIC packages.

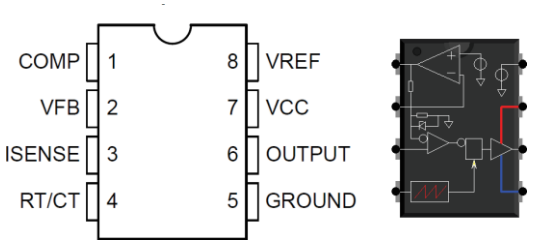


Figure 3.b – SOIC and PDIP package pin layout and CASPOC symbol

3.1 Supply voltage

The required supply voltage depends on the IC variant. Table 3.1 lists the turn-on and turn-off thresholds of the undervoltage lockout (UVLO), together with the maximum duty cycle. The UC3844 and UC3845 are limited to 50%, which makes them suitable for applications such as half-bridge control or limiting the on-time of a flyback converter.

Table 3.1: Under Voltage Lock Out [UVLO] and maximum duty cycle

Type		UVLO On	UVLO Off	Max dutycycle
UC3842A		16.0*V*	10.0*V*	< 100%
UC3843A		8.5*V*	7.9*V*	< 100%
UC3844A		16.0*V*	10.0*V*	< 50%
UC3845A		8.5*V*	7.9*V*	< 50%

3.2 Reference voltage

The UC3842 comes with an internal reference voltage to feed the oscillator charging. The first test is to measure if pin[8] V_{ref} gives 5 volt. The reference voltage is used to charge the timing capacitor C_T via R_T, as we will see in the next section.

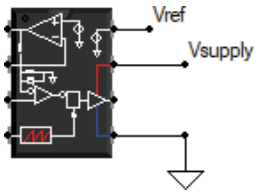


Figure 3.2.a – Supply voltage and reference voltage Vref

Our first goal is to see if the UC3842 is active and this is done by measuring the reference voltage on pin[8].

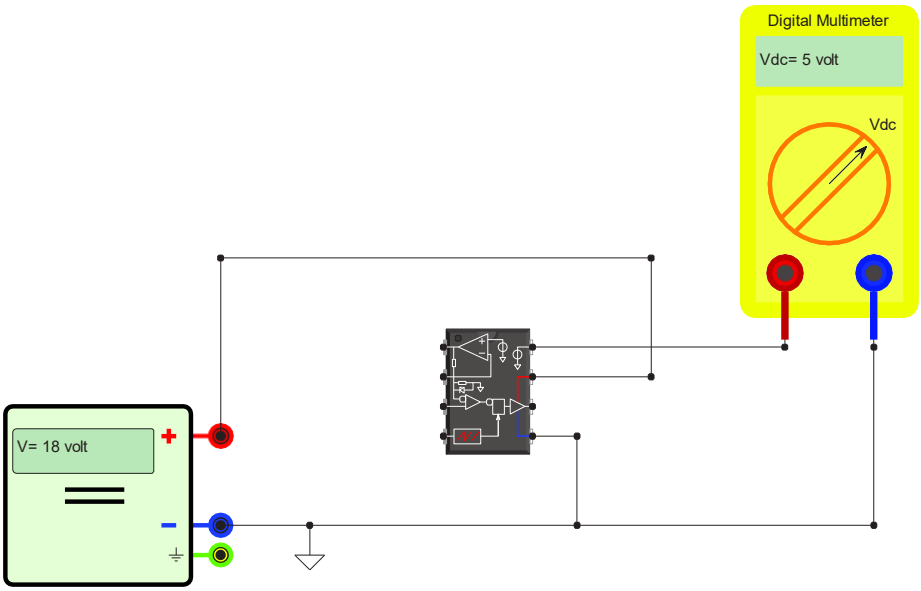


Figure 3.2.b – Measure Vref on pin[8]

Build the circuit and connect the power supply. Increase the supply voltage from 0 volt to 20 volt, and observe at which supply voltage level, pin[8] V_{ref} gives 5 volt.

Table 3.2.a – V_{ref} as function of V_{supply} for increasing supply voltage

Supply voltage V_{supply}	Reference voltage V_{ref}
0	0
5	.
10	.
15	.
16	.
17	.
18	.
19	.
20	.

Decrease the supply voltage from 20 volt to 0 volt, and observe at which supply voltage level, pin[8] V_{ref} gives 5 volt. Fill in the three boxes in Figure 3.2.c, to mark the on and off of the UC3842.

Table 3.2.b – Vref as function of Vsupply for decreasing supply voltage

Supply voltage V_{supply}	Reference voltage V_{ref}
20	.
19	.
18	.
17	.
16	.
15	.
14	.
13	.
12	.
10	.
5	.
0	.

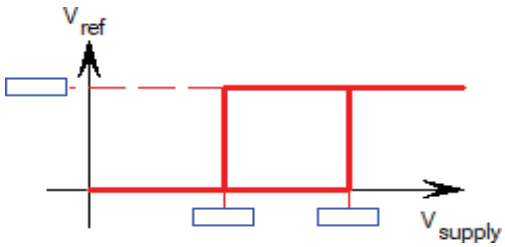


Figure 3.2.c – Measure the hysterese of Vref depending on the supply voltage Vsupply

3.3 Internal oscillator

The IC switching frequency is set by an external resistor-capacitor network that is charged and discharged by the UC3842. The timing capacitor CT is charged through RT. When CT reaches its upper threshold, it is discharged internally and the cycle starts again. The oscillator controls the switching frequency and may also provide timing for constant-on-time or constant-off-time control.

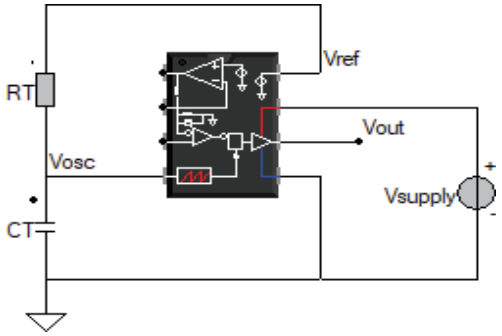


Figure 3.3.a – Basic circuit for the internal oscillator

Oscillator frequency

The oscillator is based on an external capacitor that is charged by via an external resistor and discharged whenever the maximum capacitor voltage is reached. The charging time of the capacitor is given as

$$T_{charge} = R_T \cdot C_T$$

where R_T and C_T are the external resistor and capacitor, as shown in Figure 3.3.b

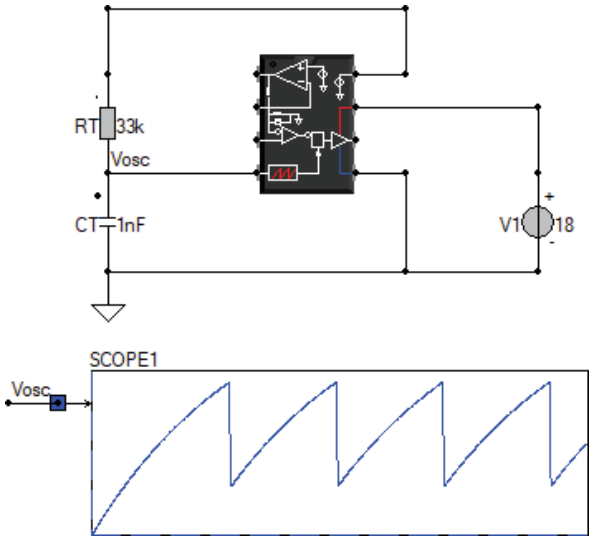


Figure 3.3.b – External resistor RT and capacitor CT define the switching frequency

The capacitor is discharged whenever the maximum voltage reaches approximately $2.7v$. However this varies among different manufacturers.
The oscillator voltage is shown in Figure 3.3.c

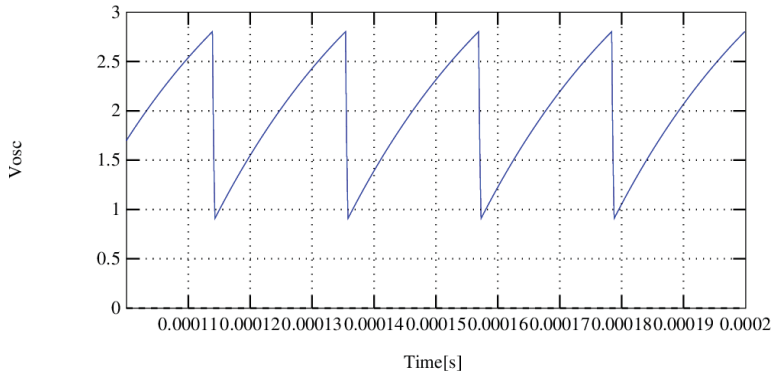


Figure 3.3.c – Oscillator voltage V_{osc}

Question:

What is the minimum and maximum value of the voltage V_{osc}.

Answer:

Maximum Voltage=[ ]
Minimum Voltage= [ ]

3.4 Timing Capacitor and Resistor

The oscillator frequency is given by the timing resistor and capacitor and is related by:

$$F_{osc} = \frac{1.72}{R_T \cdot C_T}$$

The timing capacitor and resistor can also be read from Figure 3.4

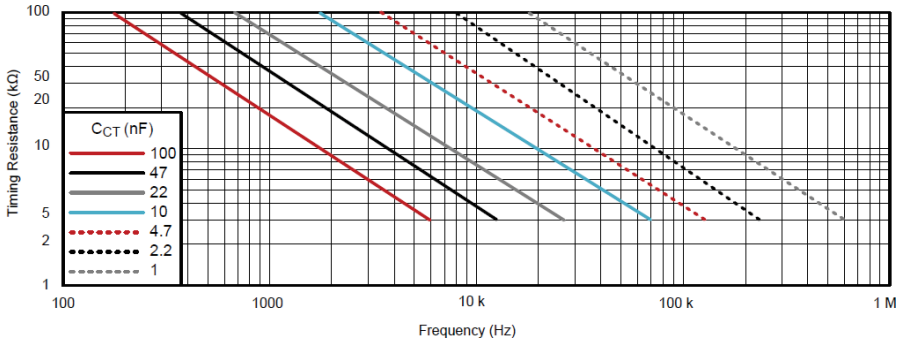


Figure 3.4 – Datasheet resistor RT and capacitor CT for defining the switching Freq.

3.5 Variable frequency

A variable frequency can be created by adding a variable resistor in series with the timing resistor R_T, see Figure 3.5. Use a variable resistance of $100k\Omega$ in series with a fixed resistance of $15k\Omega$, to ensure a minimum frequency defined by the fixed resistor. The fixed resistor R_T is is used to limit the charging current of the timing capacitor C_T If you adjust the variable resistor and measure the frequency of the oscillator voltage, the period changes depending on the total resistance, see to Figure 3.5

Question:

Build a circuit to create a adjustable frequency. Adjust the resistance and measure the oscillator frequency. Note the frequency in table 3.5.3

Answer:

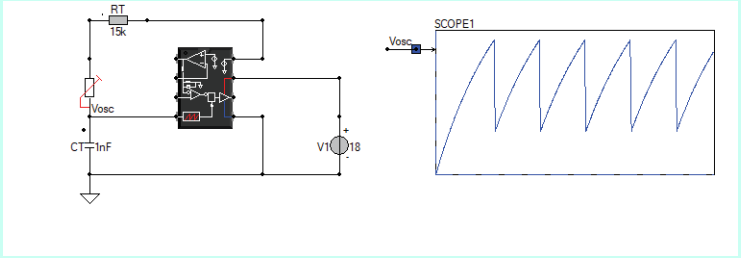


Figure 3.5 – Variable oscillator frequency, by adjusting RT

Table 3.5 – Frequency of V_{osc} as function of the series resistance.

Variable resistance[Ω]	Oscillator frequency[kHz]
0	.
$5k$	.
$20k$	.
$50k$	.
$75k$	.
$100k$	.

3.6 Variable dutycycle

Pin [3] *Isense* is used for implementing peak current mode control. However, we can also use it to create a variable duty cycle. As soon as the voltage on this pin crosses the reference value of V_{ref} = 1 volt, the output voltage V_{out} is set to zero volt. For a variable dutycycle control, this signal is created from the oscillator voltage $Vosc$.

Isense

The *Isense* pin is used to turn off the output as soon as the voltage on that pin exceeds 1 volt. Using Isense we can control the duty cycle. If we both measure V_{osc} and V_{out} while pin *Isense*is not connected, we have the maximum dutycycle

Question:

Measure V_{osc} and V_{out}. What is the maximum dutycycle?

Answer:

The maximum dutycycle is given by the value of C_T, as shown in Figure 3.6.a

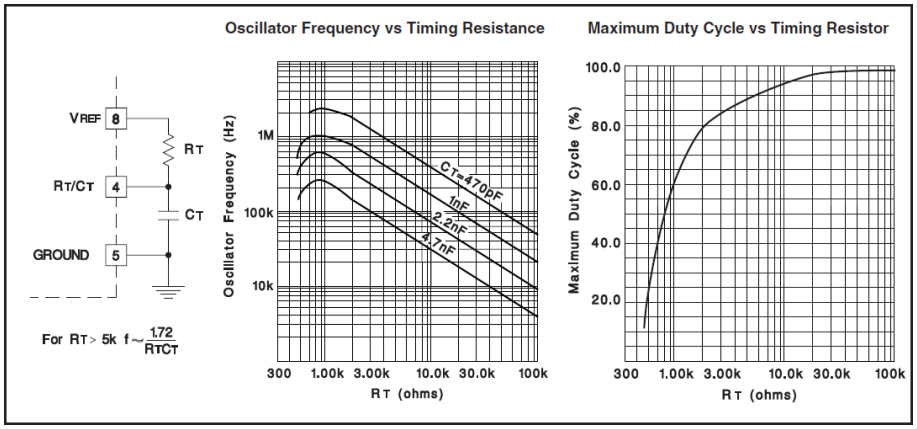


Figure 3.6.a – Oscillator Section, copyright: Datasheet Unitrode

Choose a low capacitor value C_T, in order to have a larger value for R_T, as this will result in a lower current drawn form the V_{ref} reference voltage pin[8]. Figure 3.6.2 shows the oscillator voltage and the output voltage.

Since *Isense* remains below 1 volt, the output V_{out} remains high with the maximum duty cycle, see Figure 3.6.3

The maximum dutycycle is defined by the size of the timing capacitor C_T as defined in Figure 3.6.4
If we would have a controllable signal that crosses the reference voltage of V_{ref} = 1 volt, during the on-time, we would be able to control the duty cycle. We can create this signal from the oscillator voltage V_{osc}, but this signal should bot be disturbed, in order not to influence the timing of the oscillator. Therefore we need to buffer the oscillator voltage V_{osc}.

Depending on the manufacturer of the UC3842, the minimum and maximum value of V_{osc} vary. The original UC3842 from Unitrode, varies between !.8 < V_{osc} < 3.5. In the datasheet, only the voltage amplitude of $\hat{V_o}_{sc}$ = 1.7 volt is defined. Some manufacturers have a lower minimum oscillator voltage, less than 1.7 volt. To use the oscillator voltage V_{osc} for controlling the dutycycle, we need a transistor to buffer the oscillator voltage. Unitrode recommended the circuit as given in Figure 3.6.5.

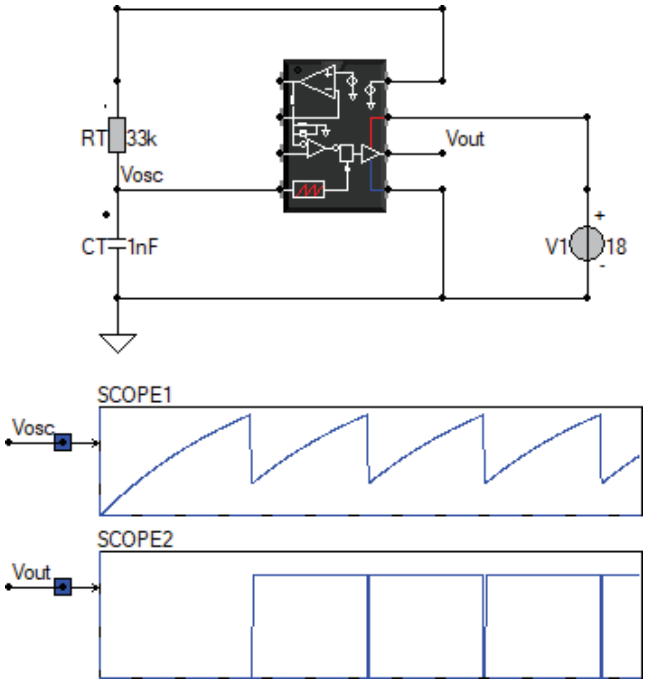


Figure 3.6.2: Maximum duty cycle

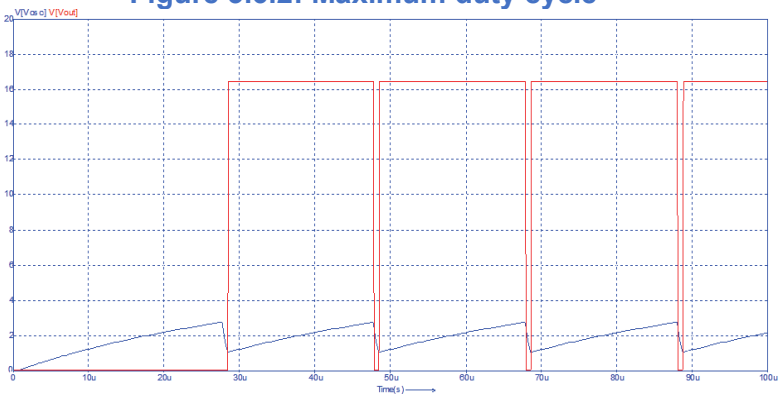


Figure 3.6.3: Maximum duty cycle

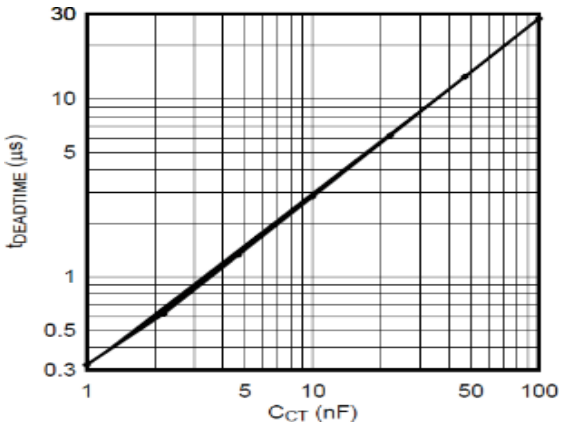


Figure 3.6.4: Maximum duty cycle given in µs as function of the timing capacitor CT

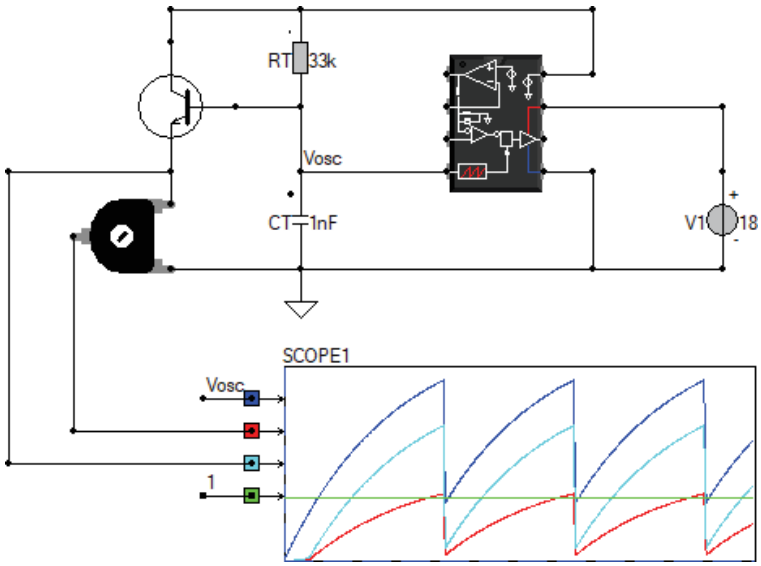


Figure 3.6.5: Buffering the oscillator voltage to derive a control signal for variable duty cycle.

The voltage at the *Isense* pin[3] is approximately 0.7 volt less the oscillator voltage V_{osc}. If the minimum voltage of V_{osc} is less than 1.7 volt, the maximum possible voltage at *Isense* at the beginning of the period is also less than 1 volt, due to the voltage drop V_{be} = 0.7 volt of the NPN transistor. Therefore it will not be possible to have a duty cycle of 0%

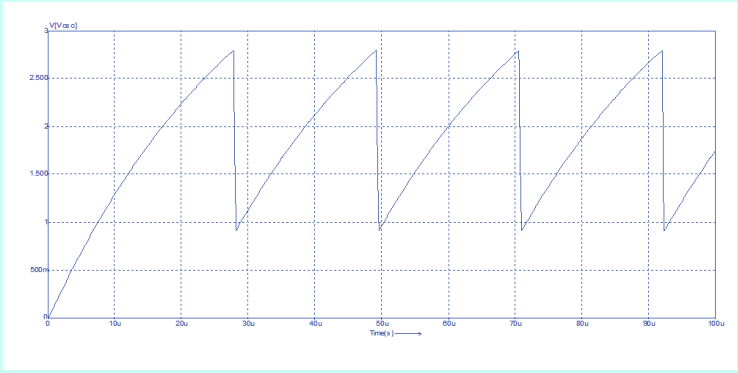
A second PNP transistor is required to shift the level of the oscillator voltage above the reference voltage of 1 volt. Therefore we are using a second PNP transistor to increase the voltage level. A PNP transistor is first buffering the oscillator voltage and because of the V_{be} = 0.7 voltage drop, the oscillator voltage is now increased by 0.7 volt, see Figure 3.6.6.

Question:

Measure V_{osc} and write down the maximum and minimum voltage.

Answer:

V_{osc}^{max} = [ ]
V_{osc}^{min} = [ ]



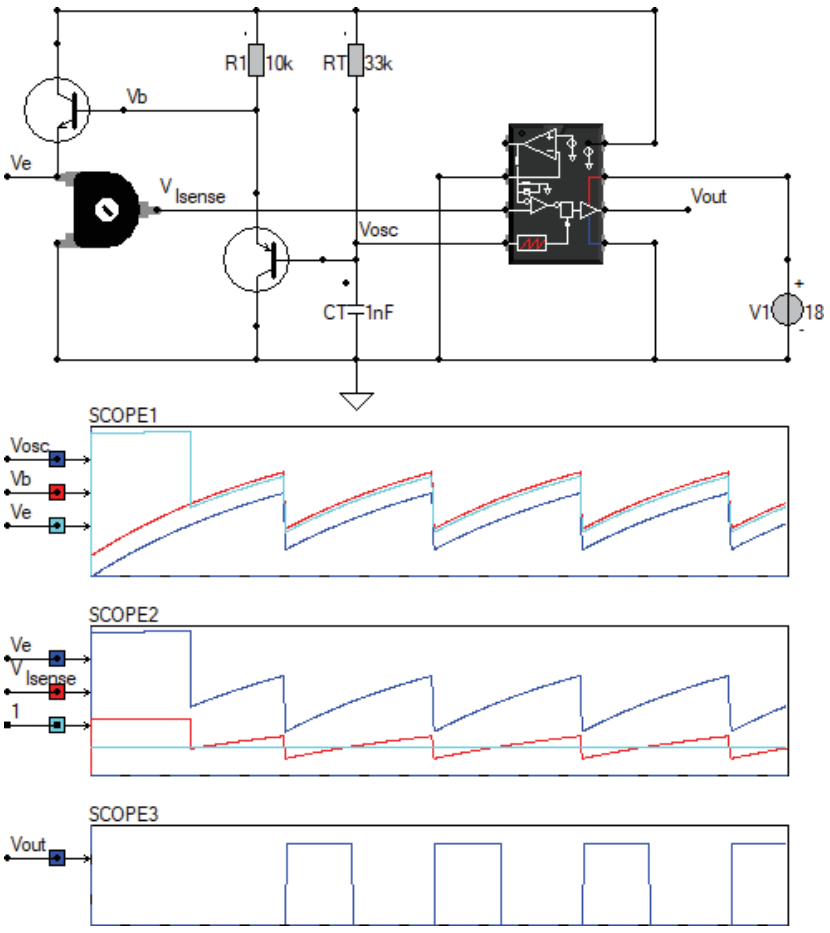


Figure 3.6.6: A PNP transistor used for buffering V_{osc} and increasing the voltage level by 0.7b

4 Building and Measuring Current Limiting Flyback (WEEK 4)

Build the current-limited flyback converter shown below on a breadboard. Use the unchanged CASPOC model below as the reference for topology, component connections and expected behaviour. The output capacitor may be selected by the student from the lecturer-approved components.

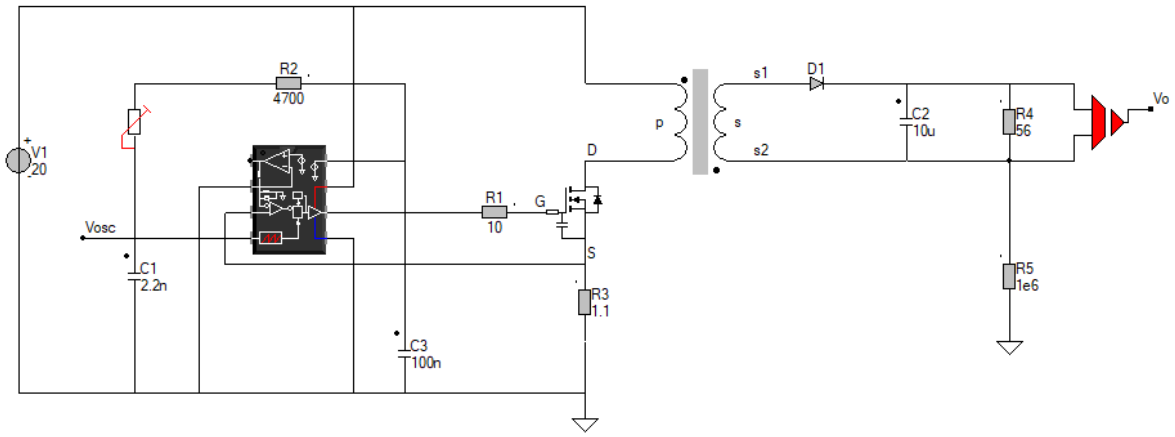


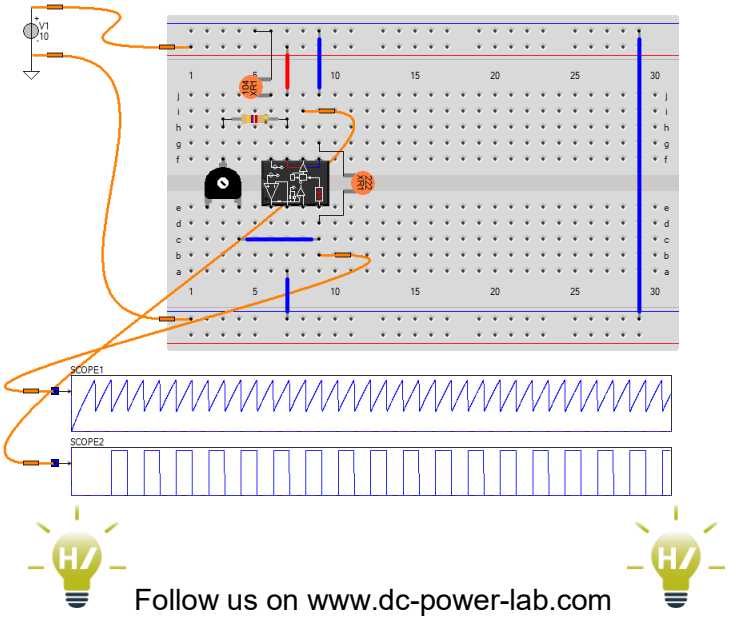
Figure 4 – Reference topology of the UC3845 current-limited flyback converter

Reference value	Implementation
Input supply	20 V, with current limit enabled
Controller	UC3845; pin 2 grounded and pin 1 left open
Transformer	Lp = Ls = 150 µH; Np:Ns = 1:1
Current sense	2 × 2.2 Ω in parallel (approximately 1.1 Ω)
Timing network	CT = 2.2 nF; adjustable RT = 4.7–14.7 kΩ
Initial load	560 Ω
Output capacitor	10uF

LECTURER CHECK BEFORE POWER-UP The lecturer must inspect the breadboard, supply current limit, component polarity and probe-ground connections before the circuit is energised.

4.1 Build and Photograph the Breadboard Circuit

First construct the complete circuit using short connections around the UC3845, see example below of a breadboard simulation below:



After checking the oscillator add the power stage of the flyback, so the MOSFET, gate resistor, transformer, output capacitor and current-sense resistor.

Take two photographs of the same completed circuit:
A. Figure 4.1.a – Top view breadboard flyback
B. Figure 4.1.b – Side view breadboard flyback

4.2 Oscillator and Gate-Drive Verification

With lecturer approval, energise the circuit. Display the UC3845 timing-capacitor signal at pin 4 and the gate-drive pulse at pin 6 simultaneously. Adjust RT until the switching frequency is approximately 100 kHz.

Save one complete oscilloscope screen directly to a USB drive using the full-screen image-export function. Enter the unique code in the top-left corner using the oscilloscope text/annotation function before saving. The code must be part of the original export and may not be added afterwards.

Add the original export as:
A. Figure 4.2.a – Oscillator ramp of the flyback on the scope.
B. Figure 4.2.b – Gate-drive pulse of the flyback on the scope.

Awnser:
C. Determine the switching frequency and gate-pulse duty cycle both Channel 1 & Channel 2 explain whether their timing relationship is consistent.
Response:

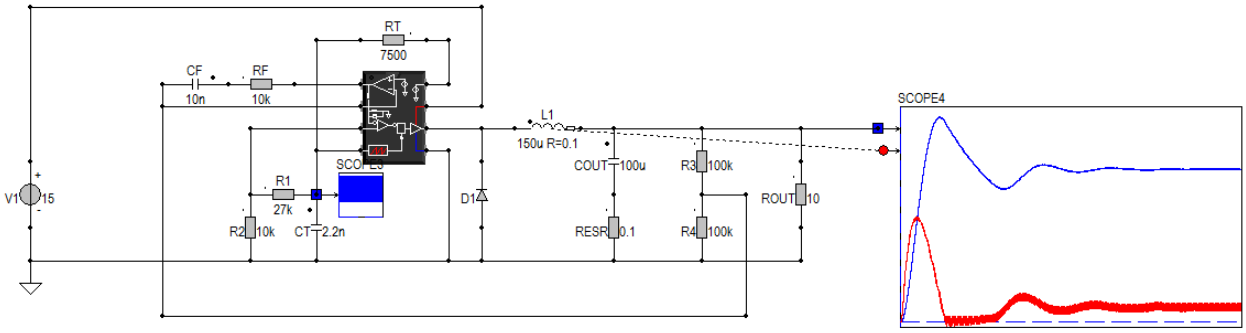
4.3 Output-Voltage Start-Up Transient

Keep the initial load at 560 Ω. Configure the trigger to capture the output voltage from before switch-on until it has reached steady state. Use the lecturer-approved probing method.

Add the original export as:
A. Figure 4.3.a – Output voltage of the flyback on the scope.
B. Figure 4.3.b – Start-up voltage of the flyback on the scope.

5 Building and Measuring a Closed-Loop Buck Converter(WEEK 5)

Build the circuit shown below on a breadboard. Use the CASPOC model as a reference for circuit topology, component connections and expected behaviour.



After completing the circuit, operate the converter and reproduce the blue output-voltage waveform shown in the CASPOC simulation. Compare the simulated behaviour with the behaviour of your physical circuit.

All photographs and oscilloscope captures must originate from your own laboratory session. At the beginning of the lesson, the lecturer will provide a unique session code. This code must be visible in the required photographs and oscilloscope exports.

5.1 Top View of the Breadboard Circuit

Take a clear top-view photograph of your complete closed-loop buck converter.

The photograph must:

- show the complete breadboard and circuit;
- be sufficiently sharp to inspect the wiring and component placement;
- show the input, output and measurement connections;
- show the unique session code in the bottom-left corner of the photograph.

The session code must be physically present when the photograph is taken, for example on a small card placed next to the breadboard. It may not be added to the photograph afterwards.

Add the photograph to your report as: *Figure 5.1 – Top view breadboard buck*

5.2 Side View of the Breadboard Circuit

Take a clear side-view photograph of the same closed-loop buck converter.

The photograph must have the same requirements as 5.2

Add the photograph to your report as: *Figure 5.2 – Side view breadboard.*

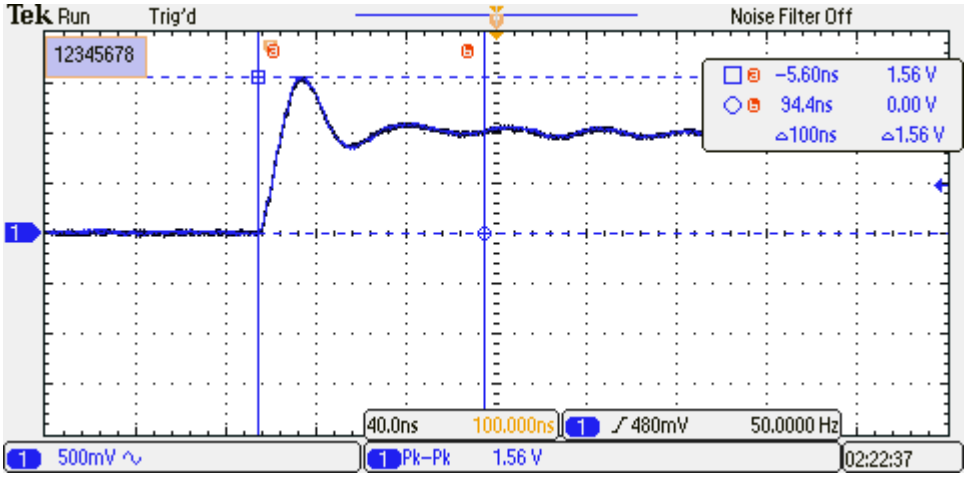
5.3 Output-Voltage Start-Up Transient

Before switching on the converter, record the following predictions:

A. *Predict the expected steady-state output voltage.*
B. *Predict whether the output voltage will initially rise or fall.*
C. *Predict whether the start-up response will contain overshoot, undershoot or oscillation.*
D. *Estimate the time required for the output voltage to reach steady state.*

Do not change these predictions after performing the measurement. Corrections and explanations may be added separately after the measurement.

Configure the oscilloscope trigger function to capture the complete output-voltage start-up transient. The capture must show the output voltage from before switch-on until steady-state operation has been reached.



Before saving the image, enter the unique session code provided by the lecturer in the top-left corner of the oscilloscope display using the oscilloscope's text, label or annotation function (see top scope export as reference). The code must be present in the original oscilloscope export and may not be added to the image afterwards. Save the complete oscilloscope screen directly to a USB drive using the oscilloscope's full-screen image-export function.

<u>The exported image must clearly show:</u>

- the complete start-up waveform;
- the unique session code;
- relevant oscilloscope measurements and cursors.

Add the original oscilloscope image as: *Figure 5.3 – Measured output-voltage start-up.*

<u>Using only the information visible in Figure 5.3, determine:</u>

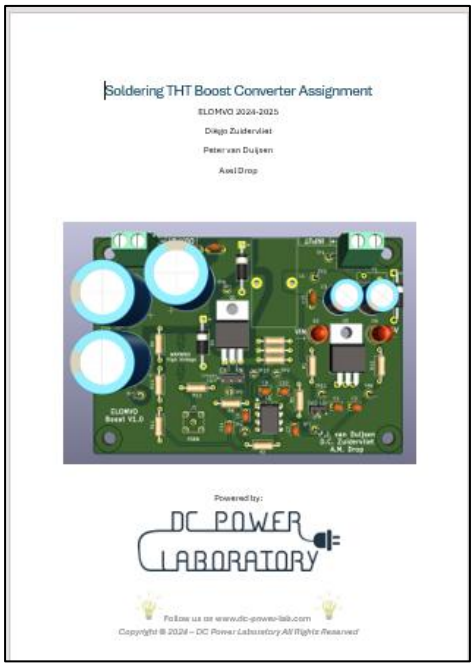
E. *the time required to reach steady state;*
F. *the maximum output voltage Vp-p;*
G. *the steady-state output voltage.*

H. Compare the measured response with your original prediction. Explain any observed overshoot, undershoot, oscillation or difference in settling time. And let the lecturer sign this chapter in the system.

6 Soldering the Boost Converter (WEEK 6)

In this part of the laboratory course, you will assemble a boost converter PCB. Choose either the SMD or THT track. The THT Track will have more measurement questions, but with a less complex circuit board to solder. The SMD track will have less measurement questions, but for soldering you will need more skills. Choose based on what skill you want to gain knowledge.

The separate assembly handout for your selected track contains the schematic, PCB layout, BOM and component-specific mounting instructions.



SMD Track (Easy)

SMD Track (Medium)

Both PCB versions are intended to produce comparable electrical behavior. The PCB, components and applicable assembly handout will be provided during the lab sessions.

6.1 ESD and Safe Handling

MOSFETs and other semiconductor devices can be damaged by electrostatic discharge (ESD), even when no visible spark is present. Wear a grounded ESD wrist strap, work on an antistatic mat and keep components in their ESD-safe packaging until required.

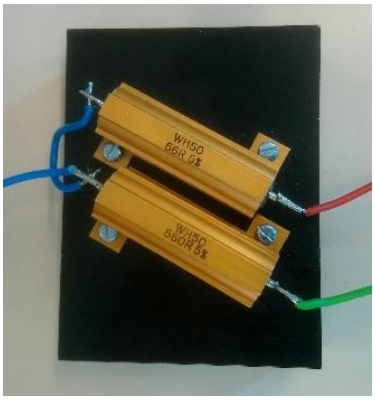
6.2 Preparing the Circuit for Measurement

Warning: incorrect component placement, poor soldering or incorrect wiring may cause a short circuit, component failure or dangerously high voltage. Wear safety glasses from this point onwards and do not energize the PCB until it has been checked by the lecturer.

Connection procedure:

Use suitable leads to connect the power supply to Vin and Vsupply. Check polarity before making the connection.

Connect the specified power resistor as the load.
- No load may allow the output voltage to rise to a dangerous level.
- A resistance that is too low may cause excessive current and component damage.



Use a T-piece to route the generator signal to both the PCB pulse input and an oscilloscope channel.

Connect the function generator to the pulse input using leads that cannot accidentally short adjacent terminals.

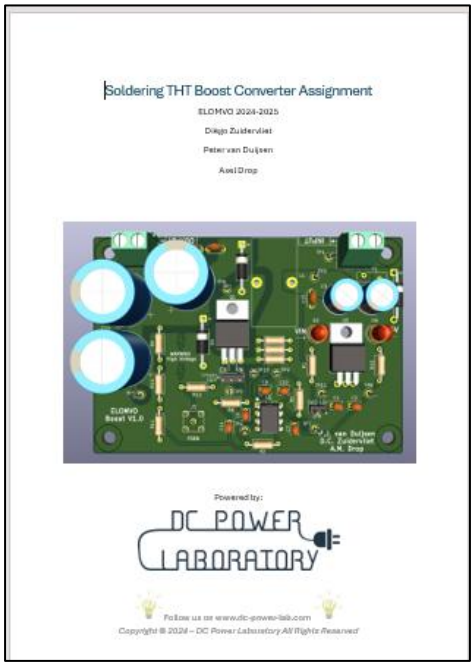
Connect a multimeter across the load to measure the DC output voltage.

Use an oscilloscope channel to observe the output waveform only when the probe and instrument voltage ratings are sufficient.

Before power-up, verify component orientation, solder quality, wiring, probe-ground locations, generator settings, load value, power-supply voltage and current limit. The lecturer must approve the complete setup before it is energized.

7 Boost Converter Measurements (WEEK 7)

Use the separate measurement assignment supplied for your chosen PCB track. The general measurement rules below apply to both versions.



SMD Track (Easy)

SMD Track (Medium)

Both PCB versions are intended to produce comparable electrical behavior. The PCB, components and applicable assembly handout will be provided during the lab sessions.

8 Feedback

Please provide a short piece of feedback about the entire course. Your comments will help us to improve the practicum for future students.

Feedback is optional, but highly appreciate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